

# 74LVC06A-Q100

Hex inverter with open-drain outputs

Rev. 1 — 14 May 2013

Product data sheet

## 1. General description

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The 74LVC06A-Q100 provides six inverting buffers. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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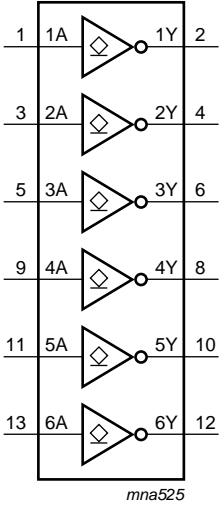
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- 5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )

3. Ordering information

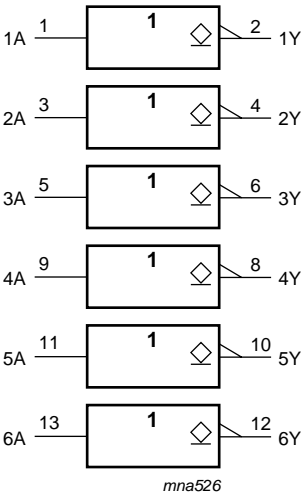
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC06AD-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC06APW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC06ABQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

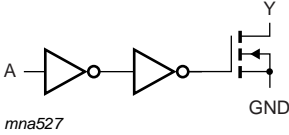
4. Functional diagram



**Fig 1. Logic symbol**



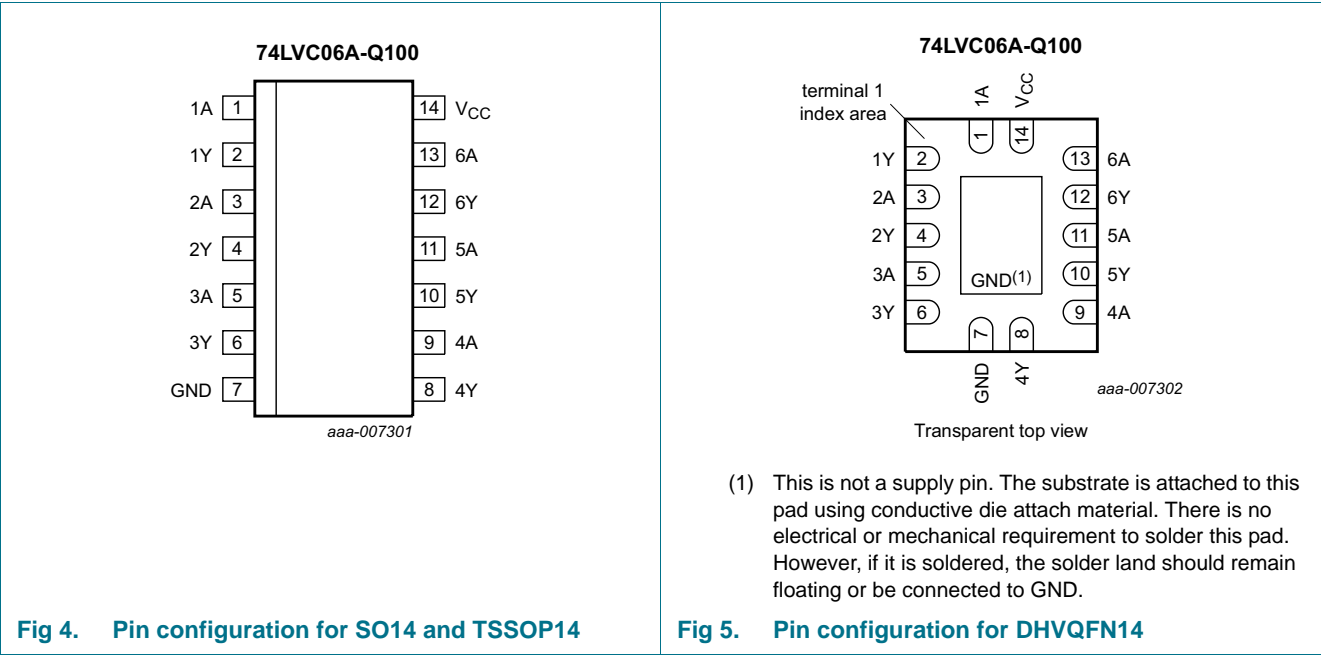
**Fig 2. IEC logic symbol**



**Fig 3. Logic diagram for one gate**

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

6. Functional description

Table 3. Function selection [1]

Input	Output
nA	nY
L	Z
H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O < 0$	-50	-	mA
$V_O$	output voltage	active mode	[2] -0.5	+6.5	V
		high-impedance mode	[2] -0.5	+6.5	V
$I_O$	output current	$V_O = 0\text{ V to }V_{CC}$	-	50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	active mode	0	-	5.5	V
		high-impedance mode	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	0.7 × V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.30 × V <sub>CC</sub>	-	0.30 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	-	-	-	-
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.20	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.6	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.3	-	0.75	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	±0.1	±5	-	±20	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V	-	±0.1	±10	-	±20	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	±0.1	±10	-	±20	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	0.1	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 5.5 V	-	5	500	-	5000	µA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 5.5 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nA to nY; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	9	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	2.8	5.7	0.5	6.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.9	3.1	0.5	4.0	ns
		V <sub>CC</sub> = 2.7 V	0.5	1.8	3.9	0.5	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.8	3.7	0.5	5.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7	1.5	2.5	0.7	3.5	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nA to nY; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 1.2 V	-	10	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	2.6	5.7	0.5	6.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.4	3.1	0.5	4.0	ns
		V <sub>CC</sub> = 2.7 V	0.5	2.6	3.9	0.5	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.2	3.7	0.5	5.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.6	1.5	2.6	0.6	3.5	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[2]</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	6.5	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	6.9	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	7.2	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

11. Waveforms

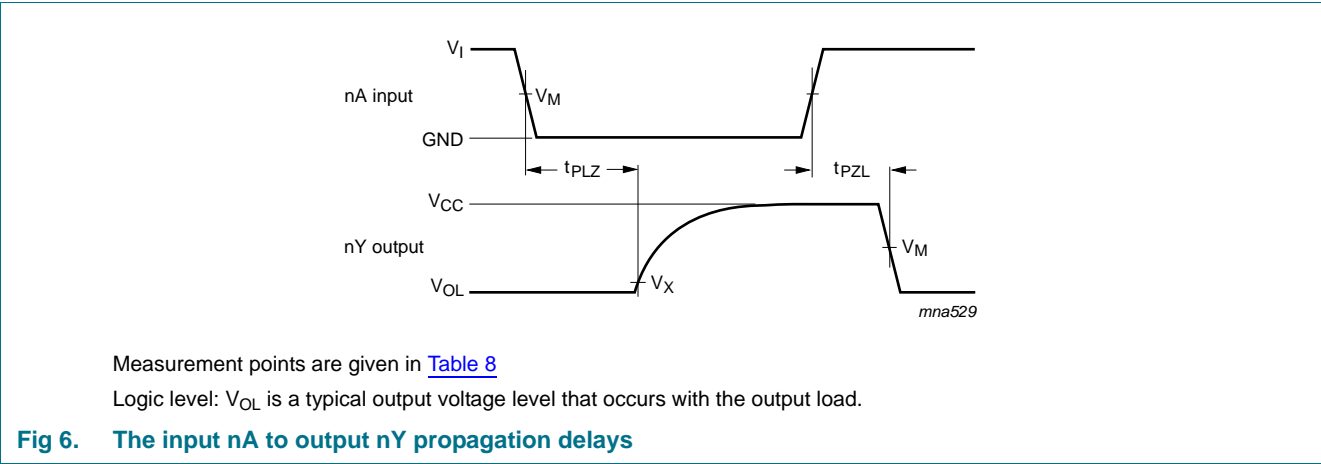
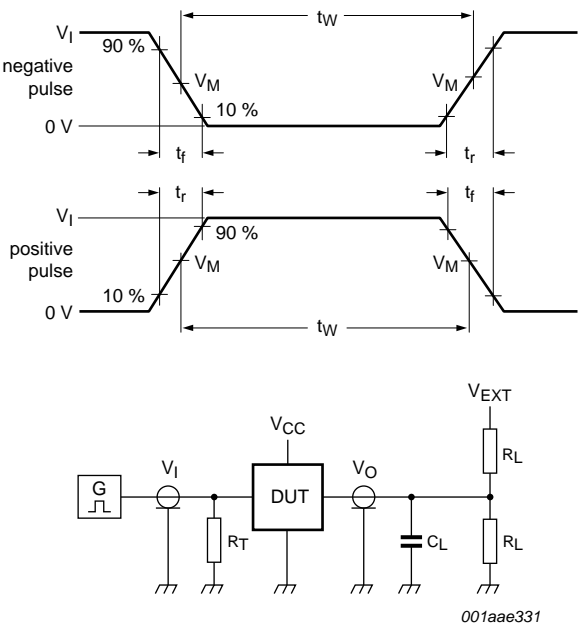


Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_X$
$< 2.7\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$
$\geq 2.7\text{ V to } 3.6\text{ V}$	$1.5\text{ V}$	$V_{OL} + 0.3\text{ V}$
$\geq 4.5\text{ V to } 5.5\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 7. Load circuitry for switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND



12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

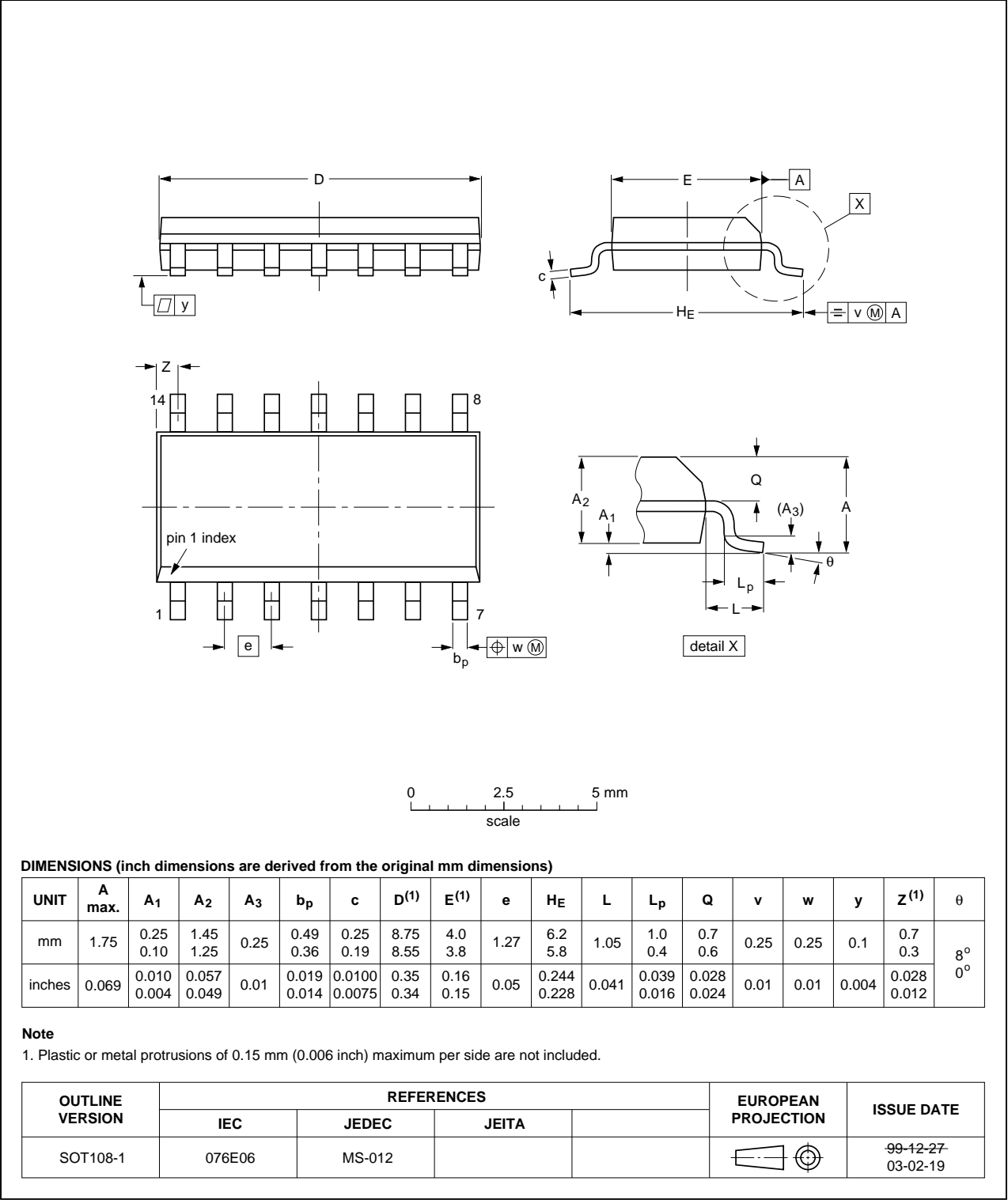


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

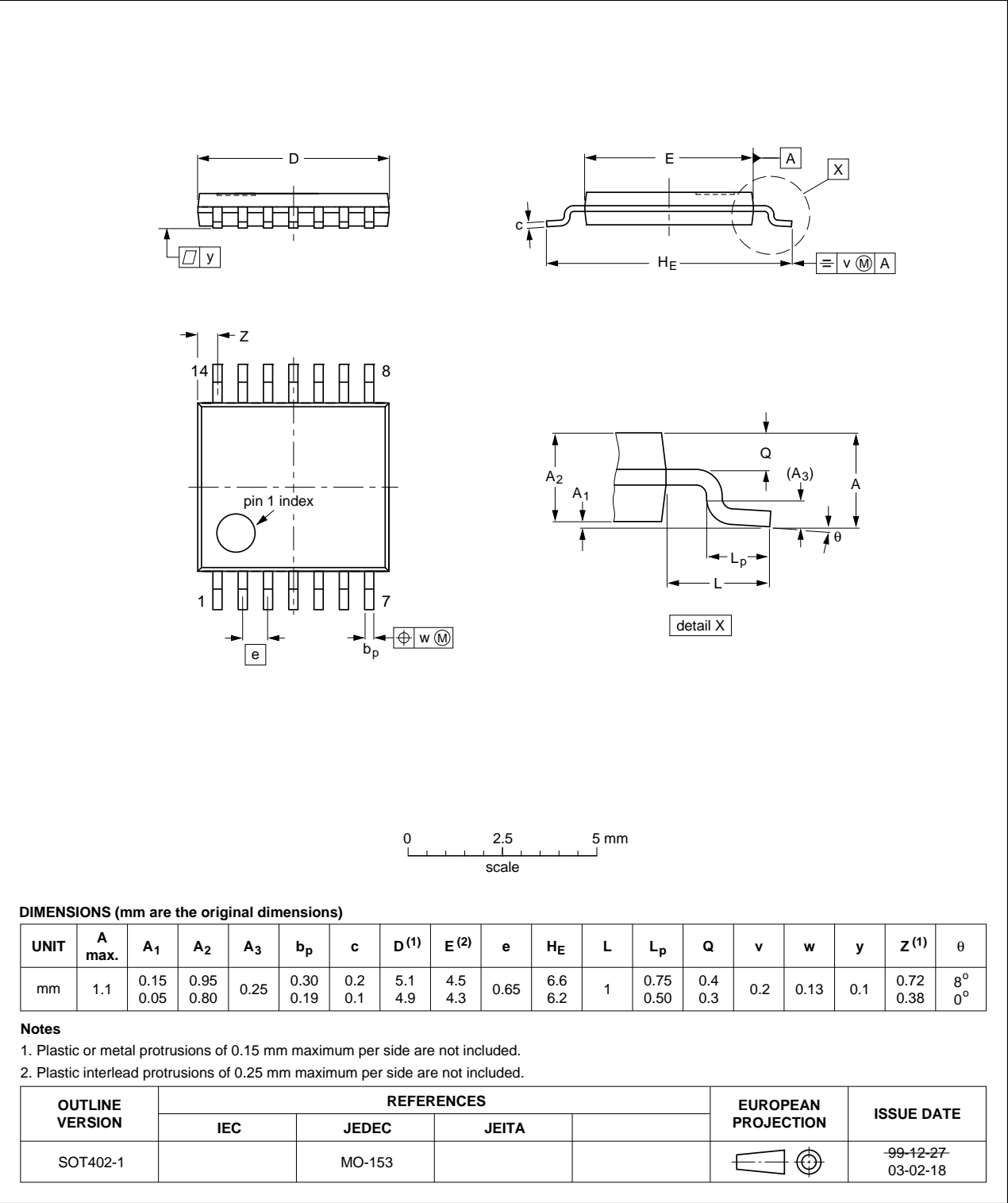


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

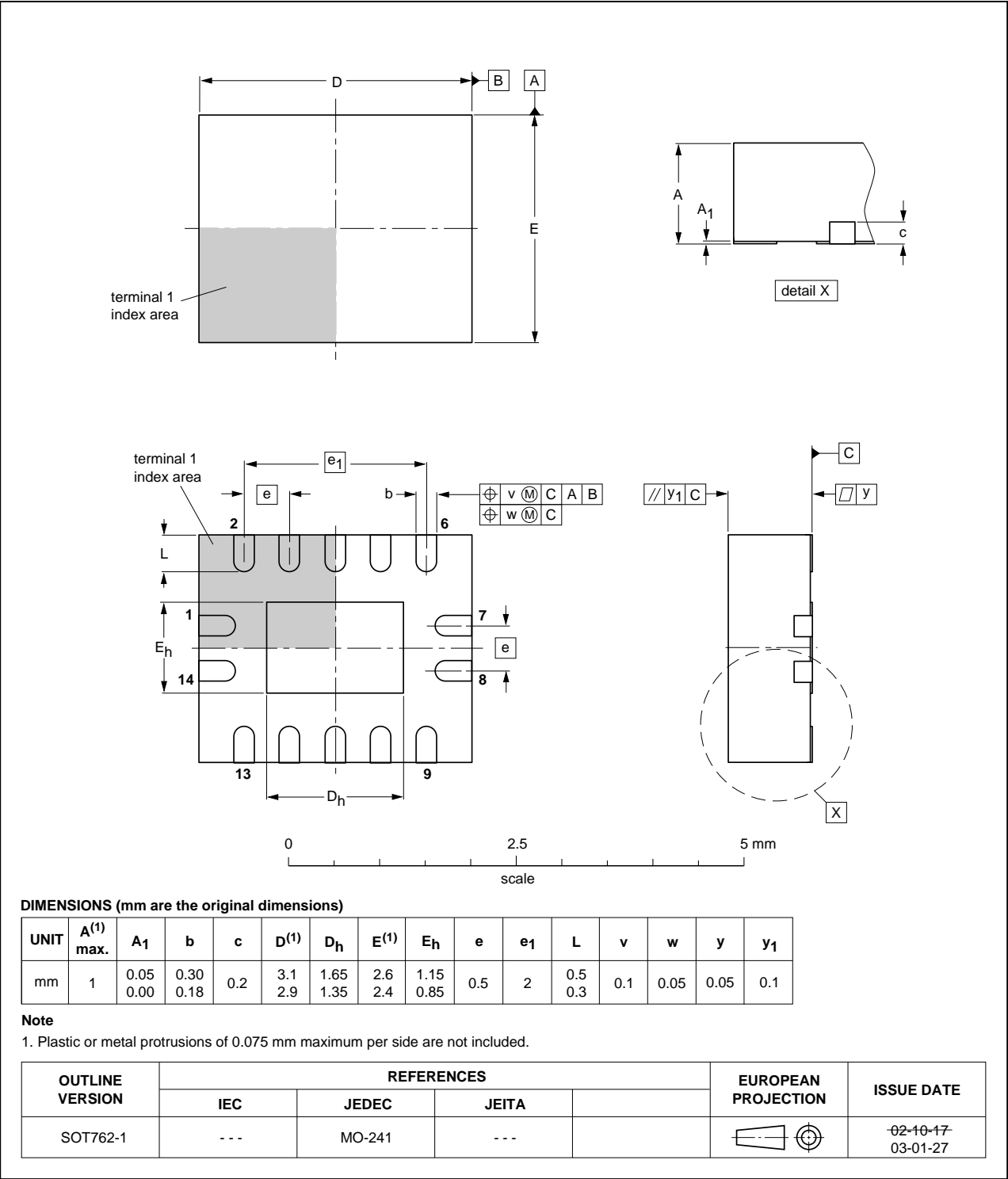


Fig 10. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC06A_Q100 v.1	20130514	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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